ABSTRACT

A memory array architecture suitable for variable resistance memory that mitigates sneak path and associated problems by limiting the number of memory cells associated with an addressed cell to a known number having a sneak path resistance that can be calculated and taken into consideration when sensing the addressed memory cell. Blocks of memory cells are associated with access transistors, which separate the memory cells connected thereto into one half (1/2) sections of cell blocks. The access transistors can be associated with n memory cells, where n is an even number of at least 2; there may or may not be an equal number of cells on either side of the transistor. The memory array has memory cells, which are grouped into 1T-2nCell blocks.